Applicants respectfully traverse the rejection of claims 1-15 and 19 as follows.

Address pointers have been used, perhaps since the beginning of the microprocessor age, if not earlier. Address pointers are typically used to access data (which may include instructions) at a particular address in memory. Hence, when the address pointers are moved, they are typically moved from one address to the next, each address aligned (or associated) with a number of data bits in the memory. The address pointers may jump from one address to a non-adjacent address, but regardless of the distance between the memory locations corresponding to the addresses, the address pointers still jump to a single address aligned with a number of data bits in the memory.

For example, in a 16-bit system, an address pointer would typically point to the address in memory where 2 bytes (16 bits) of data are stored. Further, in 32-bit and 64-bit systems, an address pointer would typically point to the address in memory where 2 words (32 bits) and 4 words (64 bits) of data are stored. For example, one of the advantages of using a 32-bit system instead of a 16-bit system, of course, is that twice as many data bits can be accessed in parallel simultaneously using a single address over a data bus that can be twice as wide.

In exemplary embodiments according to the present invention, a read pointer can be placed at a location within a data portion that is aligned with a particular address. For example, the read pointer in the present invention can be placed at a first non-blanked out pixel in the portion of graphics data aligned with the start address. Using such read pointer that can be placed at a location after one or more pixels at a beginning of the portion of the graphics data aligned with the start address, such one or more pixels can be blanked out. Hence, the read pointer of the present invention is more than a mere address pointer used to point to an address. Instead, it can flexibly

point to a location within the data aligned with a particular address. For efficient transfer of data, all of the data aligned with that particular address may be transferred concurrently over a parallel data bus, however, the read pointer can be used to blank out one or more pixels by pointing to a first non-blanked out pixel of the data aligned with that particular address.

For example, FIG. 15 of the present application illustrates that a read pointer 602 is placed after a first pixel (e.g., first 8 bits) 604 of a 32-bit word 600 that is aligned with the start address. The first pixel is blanked out, and the remaining three 8-bit pixels are effectively shifted to the left by one pixel. Prior to blanking out, the read pointer 602 points to the first bit of the 32-bit word. After blanking out, the read pointer 602 points to the ninth bit of the 32-bit word. (FIG. 15, page 61, line 30 through page 62, line 6). This shows that the read pointer in this exemplary embodiment of the present invention can be flexibly placed at any pixel within the 32-bit word aligned with the start address, where the start address is used to access all 32 bits of data aligned thereto. As such, a read pointer that can flexibly point to a location within a data portion aligned with an address, and not merely pointing to that address, is important to the present invention.

Tateyama appears to disclose a method of smoothly scrolling an image horizontally. (col. 9, lines 34-38). However, "according to the invention [in Tateyama], timings for reading and transmitting data are controlled to perform a horizontal scroll." (col. 9, lines 34-36). In fact according to Tateyama, "The read-timing is shifted in order to realize a horizontal scroll. The amount of the shift varies depending on whether the picture is scrolled by odd or even dots." (col. 7, lines 31-33). The figures and the passages of Tateyama cited by the Examiner (i.e. FIGs. 24A, 24D, 24E and 28, and col. 8, lines 3-26 and 50-52) and other figures and passages also confirm that

Tateyama discloses a method for horizontal scrolling based on controlling timings for reading and transmitting data.

Since the whole smooth horizontal scrolling scheme in Tateyama is based on controlling timing for reading and transmitting data, it necessarily results in a complicated system where the alignment between timing signals and data must be adjusted in order to achieve horizontal scrolling. In the present invention, on the other hand, smooth horizontal scrolling is realized simply by displaying the graphics data starting at the read pointer placed at a first non-blanked out pixel. Applicants respectfully submit that the approach taken by Tateyama is so different from the approach of the present invention, Tateyama would tend to teach away from the present invention.

To support the rejection of claims 1-20, the Examiner states that "Saeger et al. teach the position of the PIP overlay on the screen will be determined by the start address of the read pointer of the video RAM at the start of the scanning for each field of the main signal" and cites FIG. 18 and col. 16, lines 7-10 of Saeger et al. Applicants respectfully submit, however, that the read pointer disclosed in Saeger et al. appears to be nothing more than a conventional address pointer that points to an address for reading data. In the absence of any teaching or suggestion that such conventional address pointers can be used to flexibly point to a particular bit or pixel within data aligned with a start address or any other address, applicants respectfully submit that Tateyama and Saeger et al. should not be combined to reject the claims of the present application.

The Examiner also recites a passage from Sokawa et al. to support the rejection of claims 1-20. According to the Examiner, "Sokawa et al. teach a read pointer P_R pointing to the head address of the first input buffer portion, starting the read of the input image data from the first input buffer portion" and cites FIG. 12 and col. 22, lines

28-31 of Sokawa et al. However, similar to the read pointer disclosed by Saeger et al., the read pointer of Sokawa et al. appears to be a conventional address pointer that points at a particular address and not any particular bit or pixel within the data aligned with that particular address. For example, Sokawa et al. discloses "a write (W) pointer register 2054 or 2058 for supplying pointing information indicating a write address (position) in the buffer and a read (R) pointer register 2056 or 2060 for supplying pointing information indicating a read address (position) in the buffer." (Col. 21, lines 47-52). It seems clear from the above passage of Sokawa et al., that the read and write pointers disclosed therein are conventional address pointers for pointing only to addresses, and not to any particular bit or pixel of data within data aligned with a particular address.

Further, the Examiner states that "Numata teaches the address pointer (read pointer) is shifted on[e] bit leftwardly" and cites FIG. 9, and col. 6, lines 40-41 of Numata. Applicants respectfully submit, however, this appears to be a misquote. Applicants respectfully submits that Numata discloses "<u>a value ("B")</u> of the dequantization table 5 designated by the address pointer <u>is shifted one bit leftwardly (or multiplied by 2)</u>." (<u>emphasis added</u>, col. 6, lines 39-41). Hence, this passage discloses that the value ("B") is shifted by one bit, and not the read pointer. Shifting a data value left by one bit is a commonly used method for performing an efficient multiplication operation at a bit level, and applicants respectfully submit that it has nothing to do with placing a read pointer at a bit or a pixel. Applicants further respectfully submit that the address pointer of Numata also appears to be merely a conventional address pointer that points to an address of a dequantized data buffer 6 as illustrated in FIGs. 9(A), 9(B) and 9(C).

In addition, the Examiner states that "Allen et al. teach read pointers 405, 410 and 415 using to incrementally drain the three planes of the video buffer 100," and cites FIG. 4 and col. 6, lines

31-32. While Allen et al. discloses that "[t]he sequence counter is configured to detect when a final location of the sequence of memory locations has been addressed" (col. 2, lines 56-58), applicants respectfully submit that the read pointers disclosed in Allen et al. appear to be conventional address pointers that points to an address in memory. For example, claim 9 of Allen et al. recites "starting at an address in the first data plane indicated by a first read pointer." Col. 11, lines 32-33), and claim 13 of Allen et al. recites "reading video data from respective buffer addresses pointed to by a plurality of read pointers." (Col. 11, lines 64-65). Further, Allen et al. does not appear to disclose anywhere that a read pointer can be placed at a location in a portion of data aligned with an address.

As discussed above, applicants respectfully submit that the claims of the present application would not have been obvious at the time of the invention over the cited references because: 1) Tateyama discloses a complicated method for horizontal scrolling based on controlling timings for reading and transmitting data that appears to teach away from the present invention; and 2) none of Saeger et al., Sokawa et al., Numata, and Allen et al. teaches or suggests a read pointer that can be placed at a location within a data portion aligned with a start address (that is pointed to by an address pointer, for example)

Claim 1 recites, in a relevant portion, "blanking out one or more pixels at a beginning of a portion of graphics data by placing a read pointer at a location after said one or more pixels, the portion being aligned with a start address; and displaying the graphics data starting at the read pointer placed at a first non-blanked out pixel in the portion of the graphics data aligned with the start address," which none of Tateyama, Saeger et al., Sokawa et al., Numata and Allen et al., either individually or together in any combination, teaches or suggests. Therefore, applicants respectfully request that the rejection of claim 1 be withdrawn and that it be allowed.

Since claims 2-6 depend, directly or indirectly, from claim 1, they incorporate all the terms and limitations of claim 1 in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants respectfully request that the rejection of claims 2-6 be withdrawn and that they be allowed.

Claim 7 recites, in a relevant portion, "moving a read pointer to a new start address that is immediately prior to a current start address; blanking out one or more pixels at a beginning of a portion of graphics data by placing the read pointer at a location after said one or more pixels, the portion being aligned to the new start address; and displaying the graphics data starting at the read pointer at a first non-blanked out pixel in the portion of the graphics data aligned with the new start address," which none of Tateyama, Saeger et al., Sokawa et al., Numata and Allen et al., either individually or together in any combination, teaches or suggests. Therefore, applicants respectfully request that the rejection of claim 7 be withdrawn and that it be allowed.

Since claims 8-12 depend, directly or indirectly, from claim 7, they incorporate all the terms and limitations of claim 7 in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants respectfully request that the rejection of claims 8-12 be withdrawn and that they be allowed.

Claim 13 recites, in a relevant portion, "the display engine is capable of selectively blanking out one or more pixels from a portion of the raw graphics data, said portion being aligned with a start address, by placing a read pointer at a first non-blanked out pixel after said one or more pixels and within said portion," which none of Tateyama, Saeger et al., Sokawa et al., Numata and Allen et al., either individually or together in any combination, teaches or

suggests. Therefore, applicants respectfully request that the rejection of claim 13 be withdrawn and that it be allowed.

Since claims 14-15 and 19 depend, directly or indirectly, from claim 13, they incorporate all the terms and limitations of claim 13 in addition to other limitations, which together further patentably distinguish them over the cited references. Therefore, applicants respectfully request that the rejection of claims 14-15 and 19 be withdrawn and that they be allowed.

Since claim 21 recites, in a relevant portion, "in order to horizontally scroll the graphics window to the right, the read pointer is moved to a second portion of the raw graphics data aligned with a new start address, said new start address being an address that is immediately prior to the start address, and wherein the display engine is capable of selectively blanking out one or more pixels from the second portion of the raw graphics data by placing the read pointer at a first non-blanked out pixel after said one or more pixels and within said second portion," which none of the cited references, either individually or in any combination, teaches or suggests. Therefore, applicants respectfully request that claim 21 be allowed.

Since claims 22-24 depend from claim 21, they incorporate all the terms and limitations of claim 21 in addition to other limitations, which together patentably distinguish them over the cited references. Therefore, applicants respectfully request that claims 22-24 be allowed.

In view of the foregoing amendments and remarks, applicants respectfully request allowance of claims 1-15, 19 and 21-24 and an early issuance of a patent. If there is any remaining issues that can be addressed over the telephone, the Examiner is invited to call applicants' attorney at the number listed below.

Attached hereto is a marked-up version of the changes made to the above-identified application by the current amendment. The attached page is captioned "**<u>Version with markings to show changes made</u>**."

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By Jun E Jeon

Jun-Young E. Jeon
Reg. No. 43,693
626/795-9900

JEJ/sd

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

13. (Twice Amended) A graphics display system comprising:

a display engine for receiving raw graphics data and converting the raw graphics data into graphics contents; and

a direct memory access module for transferring the raw graphics data from memory to the display engine,

wherein the display engine is capable of selectively blanking out one or more pixels [~~associated with~~] from a portion of the raw graphics data, said portion being aligned with a start address, by [~~selectively~~] placing a read pointer at a first non-blanked out pixel after said one or more pixels and within said portion.

14. (Twice Amended) The graphics display system of claim 13 wherein the display engine comprises means for blanking out said one or more pixels [~~associated with~~] from said portion of the raw graphics data by selectively placing the read pointer.

15. (Amended) The graphics display system of claim 14 wherein the direct memory access module transfers the raw graphics data from memory starting at [~~a~~] the start address.

19. (Amended) The graphics display system of [~~claim 16~~]] claim 13 wherein the [~~read pointer is placed at a location of the~~] first non-blanked out pixel is a first pixel to be displayed.

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